AMENDMENTS TO THE SPECIFICATION:

Please replace para. [0023] with the following:

[00023] Figure 4A is a preferred embodiment 62a of the DPS block 62 of Figure 3. The real input signal from the IFFT 36 (with intervening processing blocks as necessary) is converted to binary and split into four parallel lines at a discrete amplitude generator 66, each of which is input into one of four stages, where each stage includes a modulator 68 in series with a constant envelope amplifier 70. While each of the amplifiers 70 are depicted as a single power amplifier, it is stipulated that each amplifier 70 may include one or several individual active devices, such as FETs, arranged in parallel. Preferably, each separate amplifier 70 is separated by each of its nearest-power amplifier stage by a fixed amount, and most preferably the fixed amount is about six dB. Each modulator 68 is coupled at its output to a power amplifier 70 of the same stage, and all modulators 68 within the preferred DPS 64a toggle in unison by the actuator 69. This is not to imply that the modulators 68 each shift in the same direction. While they may do so in certain instances, they are not bound in all cases to each shift phase in a common direction; to do so would not yield an analog output. They shift simultaneously in a direction dependent upon the amplitude to be synthesized. Preferably, the modulators 68sample the input bits at a time such that the phase of those input bits is one of only two possible input values, 0 or π. The output of each power amplifier 70 can be considered a "RF-bit", where the differential powers applied in the various stages correspond to the most significant bit MSB to the lesser or least significant bit LSB, one in each stage. The phase of each "RF-bit" is shifted according to the amplitude to be synthesized. Preferably, each modulator 68 is a continuous phase pulse amplitude modulator, continuous phase referring to smooth rather than discontinuous phase transitions between states. The shifted "RF-bits" are combined by first level power combiners 72 and second level power combiners 74 until a serial stream of "RF-bits" is assembled for output to one or more transmit antennas 54 (combining with the remaining I or Q stream is not specifically shown in Figures 4A or 4B).